Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (original): A method of maintaining execution threads in a parallel multithreaded processor comprises:

accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows of registers that are relatively addressable per thread.

2. (original): The method of claim 1 wherein multiple threads can use the same control store and relative register locations but access different window banks of registers.

3. (original): The method of claim 1 wherein the relative register addressing divides the register banks into windows across the address width of the general purpose register set.

4. (original): The method of claim 1 wherein relative addressing allows access any of the window registers relative to the starting point of a window of registers.

5. (original): The method of claim 1 further comprising:

organizing the register set into windows according to the number of threads that execute in the processor.

6. (original): The method of claim 1 wherein relative addressing allow the multiple threads to use the same control store and locations while allowing access to different windows of register and perform different functions.

7. (original): The method of claim 1 wherein the window registers are implemented using dual ported random access memories.

8. (original): The method of claim 1 wherein relative addressing allows access to any of the windows of registers relative to the starting point of the window of registers.

9. (original): The method of claim 1 wherein the register set is also absolutely addressable where any one of the absolutely addressable registers may be accessed by any of the threads by providing the exact address of the register.

10. (original): The method of claim 9 wherein an absolute address of a register is directly specified in a source field or destination field of an instruction.

11. (original): The method of claim 1 wherein relative addresses are specified in instructions as an address offset within a context execution space as defined by a source field or destination field operand.

12. (original): A hardware based multi-threaded processor comprises:

a processor unit comprising:

control logic including context event switching logic, the context switching logic arbitrating access to the microengine for a plurality of executable threads;

an arithmetic logic unit to process data for executing threads; and

a register set that is organized into a plurality of relatively addressable windows of registers that are relatively addressable executable thread.

13. (original): The processor of claim 12 wherein the control logic further comprises:

an instruction decoder; and

program counter units to track executing threads.

14. (original): The processor of claim 13 wherein the program counters units are maintained in hardware.

15. (original): The processor of claim 13 wherein the register banks are organized into windows across an address width of the general purpose register set with each window relatively accessible by a corresponding thread.

16. (original): The processor of claim 15 wherein the relative addressing allows access to any of the registers relative to the starting point of a window of registers.

17. (original): The processor of claim 15 wherein the number of windows of the register set is according to the number of threads that execute in the processor.

18. (original): The processor of claim 13 wherein relative addressing allow the multiple threads to use the same control store and locations while allowing access to different windows of register and perform different functions.

19. (original): The processor of claim 13 wherein the window registers are provided using dual ported random access memories.

20. (original): The processor of claim 12 wherein the processing unit is a microprogrammed processor unit.

21. (original): A computer program product residing on a computer readable medium for managing execution of multiple threads in a multithreaded processor comprising instructions causing a processor to:

access, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows of registers that are relatively addressable per thread.

22. (original): The product of claim 21 wherein the register set is also absolutely addressable where any one of the absolutely addressable registers may be accessed by any of the threads by providing the exact address of the register.